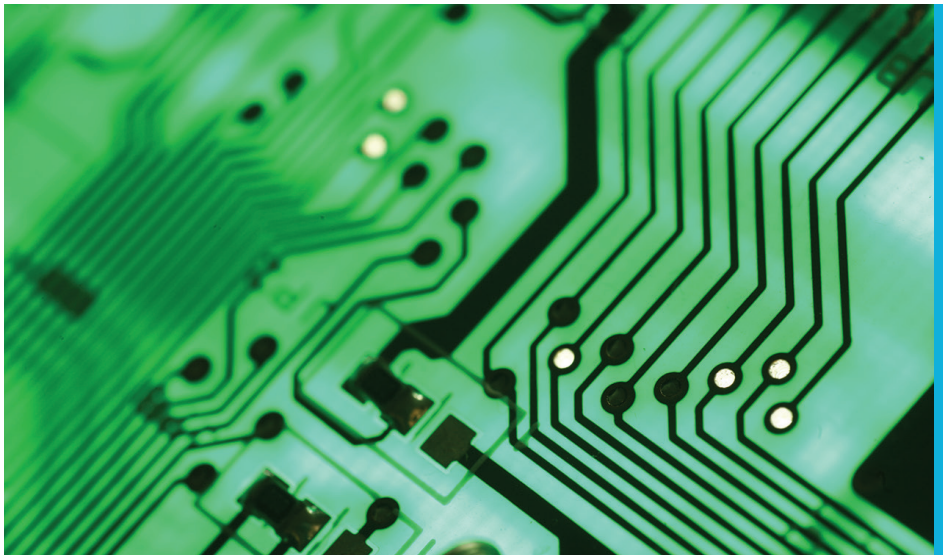

Business challenge

Verifying the designs of today's highly complex semiconductors puts great strain on limited computing resources. How can companies optimize verification and cut time-to-market for next-gen chips?

Transformation

In the semiconductor and microprocessor industries, time-to-market is everything. To help its major customers beat their rivals to market by verifying next-generation chip designs faster and more cost-effectively, Mentor worked with IBM to integrate IBM Spectrum™ LSF® scheduling technology more tightly with its Veloce emulation platform.

Business benefits

25% higher
utilization of costly compute resources with automated scheduling

Prioritizes
compute jobs more intelligently to cut end-to-end testing cycle times

Provides
advanced suspend/resume/relocate functionality to boost efficiency

Mentor Graphics

Helping bring next-gen semiconductors to market faster and more efficiently

Mentor Graphics, a Siemens business, is a leader in electronic design automation software. Its mission is to enable companies to develop better electronic products faster and more cost-effectively. With more than 5,000 employees in dozens of global locations, the company provides innovative products and solutions that help engineers conquer design challenges in the increasingly complex worlds of board and chip design.

"Using IBM Spectrum LSF, we have introduced some highly advanced capabilities in Veloce to increase utilization and efficiency."

—Vijay Chobisa, Product Marketing Manager, Mentor Graphics

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Race to value

Time-to-market is a hugely important metric in the semiconductor and microelectronics industries. Chip design and fabrication techniques improve constantly and at a rapid pace, which means that today's market-leading microprocessors will typically be out-performed by less costly alternatives within a matter of weeks. The emergence of the Internet of Things (IoT) means that next-gen processors are popping up not only in smartphones and tablets but also webcams, domestic and industrial sensors, drones, connected cars—even web-enabled refrigerators and washing machines! To succeed in this cutthroat environment, where the marketable lifespan of a new product may be measured in just a handful of months, companies must seize these limited windows of opportunity by delivering high-quality products to their customers on time.

Vijay Chobisa, Product Marketing Manager at Mentor Graphics (Mentor), comments: "Companies always want to complete the verification cycle faster even when their designs become more complex. They also have an urgent need to test more thoroughly at the design stage, because fixing problems in the fabrication stage after tape-out is too late and potentially disastrous in terms of the additional cost. In many cases, a significant bug found during the fabrication stage may mean that the entire production run is simply discarded. And some areas of the market for embedded processors are moving so fast that the sales opportunity for that particular iteration of the product may already be missed."

By finding and resolving bugs prior to the fabrication stage, microprocessor manufacturers can potentially save millions of dollars and cut time-to-market, enabling them to capture fleeting sales opportunities. However, the testing and verification phases are becoming ever more challenging because each new generation of microprocessor is more complex and has smaller, more numerous components and internal connections.

Shakeel Jeeawoody, Strategic Alliance Product Marketing, Mentor, comments: "Chip designers have long used high-performance computing grids to simulate hardware designs in software and enable them to be tested before they are physically fabricated. Our Veloce emulation platform goes a step further, providing flexible hardware that can emulate up to a two-billion gate design, such as those you might find in a GPU. Our customers achieve up to 10,000 times the performance of a conventional simulation, helping them verify their new designs faster and more thoroughly."

Naturally, the sophisticated and specialized Veloce® emulation platform is an extremely high-value resource, and Mentor's customers must try to keep it fully utilized at all times to get the best return on their investment. Put bluntly, every second that the Veloce technology is not actively running a verification scenario represents both a drag on time-to-market and a waste of dollars invested in the solution. As chip architectures have grown in complexity, and as testing teams have spread across multiple countries and time zones, it has become ever harder to ensure the optimal sharing of limited central computing resources that potentially leads to more idle periods and the corresponding wasted investment.

"Having a scheduler like IBM Spectrum LSF with the right policies in place can improve utilization of compute assets by as much as 25 percent."

—Shakeel Jeeawoody, Strategic Alliance Product Marketing, Mentor Graphics

Says Vijay Chobisa, "For many of our larger customers, the verification process involves multiple groups of users in different geographies competing for time on the emulator. Getting the balance right has become increasingly tricky, and as a result resources could be under-utilized. Our Veloce verification engine is an extremely sophisticated and powerful solution, and naturally represents a substantial dollar investment. Our customers are therefore always looking to maximize the useful work they can do on the emulator."

Using workload management software can significantly boost the effective utilization of verification resources. Internally, Mentor uses IBM Spectrum LSF for automated job scheduling on its compute resources. Shakeel Jeeawoody explains: "In our customers' experience, having a scheduler like IBM Spectrum LSF with the right policies in place can improve utilization of compute assets by as much as 25 percent."

To enable more fine-grained control over policies and better utilization, Mentor wanted to provide richer and more direct communication between Spectrum LSF and its Veloce Enterprise Server (ES) App.

By giving Spectrum LSF a direct view of the emulator hardware and the jobs running on it, Mentor could enable better and faster mapping of jobs to resources. The ultimate goal was to enable customers to execute complex test and verification processes more rapidly and thoroughly, so that they could get to market faster with higher-quality chips. As well as addressing the urgent need to beat competitors in the extremely fast-moving consumer and embedded electronics spaces, this would also ensure that customers could squeeze the maximum return out of every dollar invested in the Veloce technology.

Problems shared are problems halved

Mentor approached IBM Spectrum Computing and IBM® Systems Lab Services to expose APIs in Spectrum LSF and enable tighter integration with the Veloce platform. An IBM development team worked with Mentor to execute the development process, which ran smoothly and was completed on time.

When a new job comes in to Spectrum LSF for scheduling, the IBM software asks Veloce ES App where the job can be run, and receives several options in return. Previously, this exchange of information was somewhat opaque, but thanks to the tighter integration, Spectrum LSF now has a clear picture of what is already running on Veloce.

Vijay Chobisa notes, "Using IBM Spectrum LSF, we have introduced some highly advanced capabilities in Veloce to increase utilization and efficiency. The 'Suspend, Resume and Relocate' feature used in the integrated flow between IBM Spectrum LSF and Veloce is a great example. Imagine the emulator is fully occupied with normal-priority jobs. Ten minutes later, an ultra-high-priority job arrives. With the tight integration we now have in place, a bunch of the smaller jobs get suspended, the high-priority job is executed using the resources that have been freed up, and Spectrum LSF then resumes the suspended jobs exactly where they left off in terms of emulation time. This capability allows our customers to run high-priority jobs without needing to reserve hardware or leave other jobs waiting. And because it's highly automated, this intelligent scheduling capability also saves time and effort for the people managing the hardware resources."

The new suspend function helps Mentor's customers achieve the right balance in resource utilization. Shakeel Jeeawoody comments: "In the past, you might have a big job waiting for a long time because small jobs would rush in and take the spare capacity freed up as other small jobs finished. That issue has been addressed by this integration: if large jobs are in the pipeline, and waiting for a specified amount of time, we will look to suspend or relocate some of the resources to run that job."

He adds: "The tighter integration between Veloce and Spectrum LSF makes it easier to write the correct policies, achieve the best balance between competing jobs and get really fine-grained control over who has access to testing resources—without necessarily needing any human intervention."

Bringing next-gen tech to market faster

By enabling users of its Veloce emulation platform to take full advantage of the intelligent scheduling capabilities of IBM Spectrum LSF workload management software, Mentor is helping them save time and effort, accelerate verification cycles, maximize resource utilization and drive down time-to-market.

"Our customers are among the biggest names in the semiconductor, electronics, microprocessor, networking and telecommunications industries," says Vijay Chobisa. "As they design and deliver next-generation chips, we are helping them to seize opportunities in the market ahead of their competitors."

Shakeel Jeeawoody adds: "Chips are becoming bigger and more complex, and this means verification time is dramatically increasing with each new generation. With this tighter integration between Veloce and Spectrum LSF, customers can control access to the emulator and make sure that it is utilized for the highest-priority jobs in the most efficient way. As well as getting the most value out of their significant investments in testing hardware by ensuring that expensive equipment never sits idle, this ensures that they complete testing cycles sooner and beat their competitors to very short-lived market opportunities."

Mentor anticipates that the new integration will deliver particularly significant benefits to customers with relatively complex products and organizations spanning multiple locations.

Achieving higher utilization through more intelligent scheduling of their Veloce resources will enable faster and more thorough testing without requiring additional investments in hardware.

Vijay Chobisa concludes, "A key benefit of our work to bring Veloce and Spectrum LSF closer is the simplicity it produces. You need to make this kind of environment easy for users, who just want to submit their job and get the results quickly. Even for companies with diverse requirements and multiple different types of users, the automation and intelligent scheduling ensures that everything runs smoothly and easily with minimal need for manual intervention. This means that our customers can focus on their core objective of bringing the latest technologies to market faster and at lower cost."

Solution components

- IBM Spectrum™ LSF®
- IBM® Systems Lab Services

Connect with us

Take the next step

IBM Spectrum LSF is the leading workload manager in the electronics and semiconductor industries, used by electronic design automation (EDA) companies to run millions of jobs and save millions of dollars daily by keeping hardware resources utilized effectively. To learn more about IBM Spectrum LSF, please contact your IBM representative or IBM Business Partner, or visit the following website: **ibm.com**/systems/spectrum-computing/products/lsf/. To learn more about IBM Systems Lab Services, visit **ibm.com**/systems/services/labservices/.

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