AuvizLA Product Brief

Middleware FPGA IP for Basic Linear Algebra Subprograms (BLAS)

Auviz Systems

AuvizLA is BLAS for Xilinx FPGAs. Available in different performance levels, our Middleware IP is scalable to fit your application. The APIs for AuvizLA functions are similar to Netlib to enable an easy fit into your use model. Moreover, the IP can be used on a wide range of Xilinx devices such as the Series 7 devices, Ultrascale and Ultrascale+ devices.

Target Markets & Applications

Auviz IP is suitable for a wide range of markets spanning the breadth of embedded applications as well as the data center. Our IP serves as a key building block in a wide variety of systems.

Supported Architectures

Xilinx Series 7, Ultrascale, Ultrascale +, etc. Any board supported by Xilinx SDAccel.

Performance

AuvizLA functions are available at different performance levels to suit the application needs, and trade off resource utilization. The implementations can work all the way up to 300 MHz on a mid-speed grade Virtex-7 part. Key functions are available for Single Precision Floating Point, Half Precision Floating Point, and Fixed Point data representations. As an example, Single Precision GEMM achieves 200 GFlops on a mid-speed grade, mid-size Virtex-7 device using SDAccel.

Tool Flow

The following tool flows are supported:
Vivado HLS
Xilinx SDAccel

Availability

AuvizLA is available now in three different categories, ranging in complexity from basic to advanced. AuvizLA is licensed in different configurations, for development & for deployment.

Level 1	
amax	finds element with maximum magnitude
amin	finds element with minimum magnitude
asum	sum of absolute values of vector x
axpy	multiplies vector x by scalar a and adds to y
copy	copies the vector x into the vector y
dot	computes the dot product of vectors x and y
nrm2	computes the Euclidean norm of the vector x
rot	Givens rotation of matrix
rotg	constructs the Givens rotation matrix
rotm	applies the modified Givens transformation
rotmg	constructs the modified Givens transformation
scal	scales the vector x by the scalar α and overwrites it with the result
swap	interchanges the elements of vector x and y
Level 2	
gbmv	banded matrix-vector multiplication y = α op (A) x + β y
spmv	symmetric packed matrix-vector multiplication
trsv	solves the triangular linear system with a single right-hand-side
hemv	performs the Hermitian matrix-vector multiplication
her	performs the Hermitian rank-1 update
gemv	vector matrix multiplication
Level 3	
gemm	performs the matrix-matrix multiplication
syrk	performs the symmetric rank-k update

About us

Auviz Systems provides Middleware IP for the Data Center and Internet of Things. Auviz Systems empowers software and hardware developers through IP and custom services to integrate IP with customer designs. Auviz IP delivers higher performance, greater productivity with targeted performance optimizations.