Electrically Testing Non-underfilled Flip Chip Assemblies- Impacts on Interconnect Integrity

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Abstract— The trend towards multi-die flip chip packaging favors the incorporation of a qualified manufacturing-compatible rework process to remove and replace individual defective die. Inherent to the rework process is an electrical verification step that effectively identifies the defective device without compromising the integrity of an otherwise perfectly functional device. Unfortunately, the very feature that optimizes device integrity, that is the underfill, renders subsequent device removal extremely difficult. It is therefore desirable to investigate the behavior of various non-underfilled dies that are subjected to anticipated electrical verification conditions in order to determine whether a safe 'testing window' exists for ensuring product quality and reliability, especially considering that limited information has been published with regards to what compressive loads a non-underfilled bare die can support.

This paper presents a comprehensive study of how flip chip (100 micron diameter on 186 micron pitch), Pb-free SAC alloy interconnects behave under compressive loads applied directly to bare die that have been assembled onto an organic substrate without underfill in a multi-chip module (MCM) configuration. For various die sizes, a series of loads were examined in order to cover a vast range of possible forces used to ensure electrical contact to non-planar organic packages. Loads were applied at both ambient and elevated temperature and at both a normal angle and an artificially tilted angle.

Characterizations by load-curve analysis, co-planarity and interconnect height measurements as well as X-ray tomography demonstrated that normal angle loading induced a limited degree of deformation (<10%) that was relatively independent of temperature or load force within the wide range explored in this study. While creep behavior appeared to fall within the scope of previously published models, quantitative error analysis and subsequent best fit calculations are required to determine if the data favors any particular constitutive equation.

The artificial tilt angle was shown to induce significant deformation that, during typical test times of 20 minutes, was equally important at low or high loads with some tendency towards greater deformation at the elevated temperature. Characterizations revealed that such deformation can induce recrystallization to a finer grain structure that does not entirely revert after BGA reflow. More importantly, the more severe deformations showed evidence of interconnect cracking (ambient load) and reduced spacing (elevated temperature load) that could pose risks to package integrity.

Stress testing to 1000 DTC cycles did not induce any electrical failure for a number of simulated test conditions, but further testing with an increased sample size is recommended.

Overall, the study concludes that normal conditions of electrical testing of bare Pb-free die in advanced MCM packages will not affect the integrity of the C4 interconnects. That said, robust manufacturing controls to avert abnormal conditions such as a tilted load are deemed critical to maintaining such package integrity.

Keywords- bare die; Pb-free; C4; electrical test; MCM; rework; deformationt; creep

I. INTRODUCTION

With the advent of systems in a package (SiP) and heterogeneous integration (HI), removing and replacing one or more defective dies in a package, also known as rework, has become an important consideration for improving assembly yield and optimizing system cost. However, at the same time, packaging trends are rendering the rework process more challenging. Historically, multi-chip modules (MCM), and therefore the rework processes developed for them, have been based on ceramic substrates and lead (Pb) containing chip interconnections, often called controlled collapse chip connections (C4's). Organic substrates are becoming prevalent in light of lower cost, higher density potential, better board level reliability and general market acceptance [1]. That said, the greater coefficient of thermal expansion (CTE) mismatch between an organic substrate (17-20 ppm/°C) and the silicon chip (2.5 ppm/°C) [2] as opposed to typical ceramic substrates (6.2 ppm/°C) [3] imparts a greater stress on the interconnections. As such, underfill material between the chip and substrate has played a much greater role in mitigating thermal cycling induced failure in organic substrate based packaging. At the same time, environmental regulations have caused the chip interconnect alloy to migrate to a lead-free composition, most often comprising Sn, Ag and Cu (SAC) [4]. These SAC alloys have higher melting points (217°C or higher) as compared to the Pb-Sn eutectic [5] at 183°C, thereby imposing correspondingly higher processing temperatures. SAC alloys are also less ductile than Pb-based alloys, causing a greater amount of stress, such as that imparted by thermal mismatch, to be transmitted to more fragile regions of the interconnect system, such as the low K dielectrics of back end of line (BEOL) chip wiring [6], emphasizing again the importance of underfill reinforcement.

An integral aspect of the rework process is the need to electrically test the package and identify the defective die. The electrical test typically involves a pressure applied to the assembly at an angle normal to its major surface to ensure contact with the testing pins and an effective thermal dissipation path to accommodate die temperature increases under test conditions. From a cost and performance perspective, this pressure and heat evacuation is optimally performed in the absence of any heat spreader assembly, i.e. directly onto the bare dies of the MCM. Moreover, the bare dies under test would preferably be without underfill, since the subsequent rework processes (e.g. die removal and die replace) become arduous if not impossible [2] [7] in the presence of underfill. On the other hand, with higher power die and greater integration densities, the interconnects under test can experience temperatures far exceeding 50% of their solder alloy melting temperature ($0.5T_m$) which, under a constant load, encourages creep deformation [2] [8]. This effect would be most evident in the absence of underfill.

Successful bare die test and rework has been well documented [9] for ceramic MCM's comprising Pb-based C4 interconnections without underfill. In contrast, studies on bare die, Pb-free organic MCM rework have mostly concentrated on the impact of ambient temperature loads on underfilled die [10] [11] [12]. A previous IBM study [7] evaluated on a limited scale the effects of test loads applied to non-underfilled die on organic substrates. While encouraging, the results warrant a more thorough investigation and understanding of how electrical test variables affect chip level SAC alloy interconnect behavior at the structural and metallurgical levels. This paper reports on such an investigation where several important test parameters were considered- pressure, temperature, the number of die on the substrate and the angle of the applied force.

II. CREEP FUNDAMENTALS

A. Temperature considerations

As with most solders, SAC alloys are above $0.5T_m$ (~0.6 T_m) under the Kelvin scale at room temperature. At temperatures representative of high performance electrical test (100-120°C) these interconnects can reach almost $0.8T_m$, at which point creep behavior can be prevalent and critical [2], warranting a thorough understanding. The elevated temperature also affects alloy properties such as Young's modulus and yield strength. Nguyen, Yu and Park [13] studied the SAC305 alloy under different temperatures T and reported Young's modulus E as taking the form:

$$E(T) = 108.32 - 0.7911T + 0.013T^2. \quad (1)$$

At 25°C, the modulus is 96.7GPa while at 120°C it is only 32.1GPa. In that the solder joints and not just the bulk solder was considered, the effect of the intermetallic compounds (IMC) was taken into account, which may explain why other literature values report a lower room temperature modulus and therefore lower changes (60 GPa to 30 GPa) [14]. Fig. 1 [15] shows the temperature dependence of the yield strength for various Sn-rich alloys. While the SAC305 alloy is not specifically shown, it is evident that they all exhibit similar trends. With the SAC387 being closest in composition, it can be expected that the SAC305 yield strength would be about 48 MPa at ambient and about 12 MPa at 120°C.

B. Microstructural Considerations

The microstructure of the Sn crystal is body-centred tetragonal which is anisotropic [16]. Studies have shown that a C4 interconnect contains one or a few grains [17] [18]. Thus, the solder joint cannot be considered as a polycrystalline and the orientation of the grain is important. Moreover, it is hard to establish a general behavior of the solder joints because each joint has its own grain orientation.

SAC305 being a hypoeutectic alloy, the solder will contain three phases based on the following equations [16]:

$$L \rightarrow (S_n)_{SS} + Ag_3Sn, \quad (2)$$

$$L \rightarrow (S_n)_{SS} + Cu_6Sn_5. \quad (3)$$
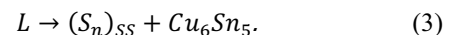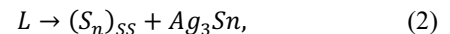
The Ag_3Sn, Cu_6Sn_5 and the eutectic phase will be present in various proportions depending upon process parameters [16] [17]. The extent to which each precipitate is present can alter the solder joint's properties.

C. Constitutive equations

With such few grains, the creep behavior of the C4's will be inter or transgranular-based rather than polycrystalline-based [17], i.e. there won't be any movement due to the grains' lattice. In this case, dislocation movement and vacancy diffusion are the two predominant mechanisms that take part in the creep behavior. Fig. 2 shows the relationship between the latter mechanisms for a SAC alloy [19]. In the low stress region, vacancy diffusion dominates, while in the high stress region it is dislocation movement that is most prevalent. Further, the curves emphasize the existence of a stress threshold where the strain rate becomes critical. This threshold, while slightly temperature-dependant, is about 10 MPa [20].

Owing to the complexity in accounting for crystal orientation for each C4, an equation considering bulk solder is mostly used. The Garofalo hyperbolic sinus secondary creep model has been used to depict a SAC305 solder without considering the intermetallic compound (IMC) regions [20] or by accounting for the Ag_3Sn precipitates at two different radii (28 nm, 30 nm) [21]:
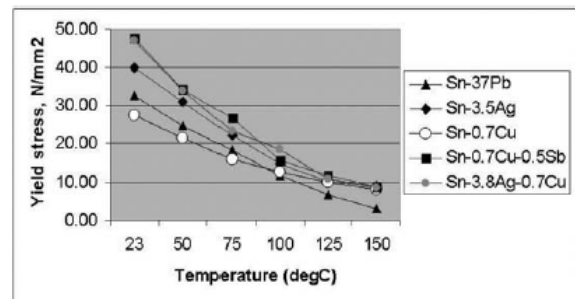

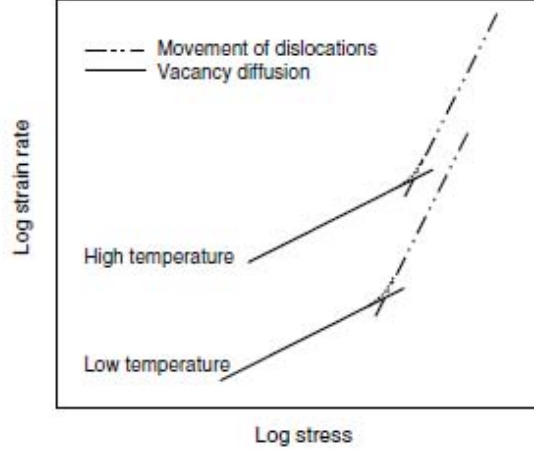Figure 1. Yield strength of various Sn alloys.

Figure 2.   Representation of creep behavior for a SAC alloy.

$$\dot{\epsilon} = A(sinh(\alpha\sigma))^n exp(-\frac{Q}{RT}). \qquad (4)$$

The Weertman two-term power law secondary creep model [20] is used to depict the different mechanisms seen in Fig.2 in a SAC305 solder, and is expressed as

$$\dot{\gamma} = A_L \left(\frac{\tau}{G(T)}\right)^{n_L} \exp\left(-\frac{Q_L}{RT}\right) + A_H \left(\frac{\tau}{G(T)}\right)^{n_H} \exp(-\frac{Q_H}{RT}), \quad (5)$$

where $\dot{\epsilon}$ is the secondary creep strain rate, $\dot{\gamma}$ is the secondary shear creep strain rate, Q is the activation energy, R is universal gas constant, T is the temperature in Kelvin, σ is the equivalent stress, τ is the shear stress, G(T) is the temperature-dependent shear and A, α, and n, are model constants. The subscripts L and H refer to low and high stress. Table I shows the model constants used in this study for the above equations.

TABLE I.   SECONDARY CREEP MODEL CONSTANTS

Model		A	Q (kJ/mol)	n	α (MPa)$^{-1}$
Garofalo without IMC		6.07	55.8	2.3	0.18
Garofalo with 28 nm radius Ag3Sn		20E3	48	5.9	0.18
Garofalo with 30 nm radius Ag3Sn		492E3	48	9.5	0.15
Weertman	low stress	11E9	39	3.4	-
	high stress	13E35	69	11	-

III.   METHODOLOGY AND EXPERIMENTAL PROCEDURES

A. Test vehicles

The test vehicles consisted of five designs corresponding to different die sizes and quantities on the same 55x55mm organic substrate. Silicon die thickness was about 0.780mm. The Pb-free solder joints were about 60μm in height and 100μm in diameter at a pitch of 185.6μm. The test vehicle design parameters are shown in Table II and the designs are illustrated in Fig. 3.

TABLE II.   TEST VEHICLE DESIGN PARAMETERS

Design	Die size (mm)	Number of dies	Number of C4 per die
1	4.22	9	436
2	8.48	4	1744
3	4.22 & 12.75	5 & 1	436 & 3924
4	17.03	1	6976
5	21.30	1	10900

B. Load tests

Compressive load tests on a bare die without underfill were performed using an Instron 8874 tool with adapted pressure heads as seen in Fig. 4. Load cells of 90.72 kg (50 lbs) and 907.18kg (2000 lbs) maximum load were used and were accurate to ±0.5%.

Five pressure heads were machined to match the corresponding chip dimensions as seen in Fig. 5. A universal shaft was used to accommodate the various pressure heads while ensuring that the load cell sensor would not heat up during the elevated temperature compressive loads.

Load tests were performed using forces up to 10.2 MPa at ambient temperature and up to 28.1 MPa at elevated temperature (120°C). Pressure was maintained for 20 minutes in order to simulate worst case electrical test conditions. Forces were applied at both a right angle (Normal test) and a slight tilt (~3.5°), based on previous studies suggesting a significant impact of such tilt [9].

Subsequent to these load tests and their interpretation, 20 samples of design number 2 were assembled and submitted to a Deep Thermal Cycling (DTC) reliability test. To reproduce typical test conditions, 6 samples were subjected to 5.4 MPa compression at 120°C for 20 minutes while 6 others were compressed at 5.4 MPa for 10 minutes at ambient then for 10 minutes at 120°C. For each of these cells, 5 parts were compressed at a normal angle while one part was compressed with a tilt angle. The other 8 samples served as controls without any test simulation.

C. Characterization methods

Non-destructive characterisations were performed before and after the compression tests in order to establish direct structural changes and therefore the impact of test-like compressions. A Fastline P300 scanning acoustic microscope (SAM) with a 100 MHz transducer and 0.5μ resolution was used to examine both C4 interfaces (chip and laminate), as well as the back end of line (BEOL) chip region comprising fragile ultra-low K (ULK) dielectric layers, for defects such as cracking or delamination.

C4 interconnection heights were measured at the edge of the die using a Mitutoyo MF-U XYZ microscope with an accuracy of 1.5μm.

An Altimet Altisurf530 confocal microscopy tool with a 3μm accuracy was used to measure the surface shape, warpage and flatness of the dies and laminates of the assemblies.

X-Ray 3D tomography was used to non-destructively characterize both exterior and interior solder bumps in their entirety or in cross-section. The apparatus used was an XTC X-Radia with 0.5μm resolution and visible volume capacity up to 60x60x60mm.
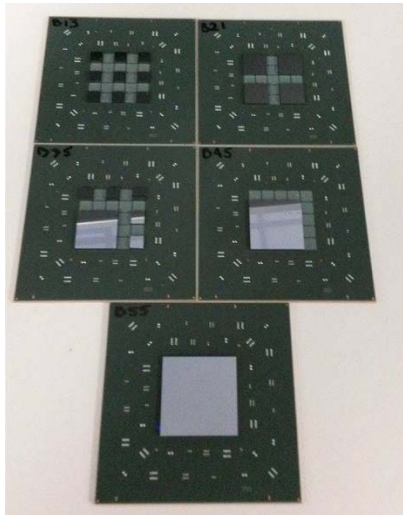

Figure 3. Test vehicle design

Figure 4. Instron 8874 use for compressive tests.

Figure 5. The five pressure heads and the shaft used in the compressive load tests.

Destructive tests were also performed to both confirm C4 heights and obtain insight into microstructural behavior. Inspection was by optical microscopy under bright field and cross-polarized light imaging. The bright field was used to visualize the global shape and measure the height of the bumps. The cross-polarized light enabled Sn grain analysis, specifically orientation, size and quantity.

The aforementioned Instron tool was also used to perform a tensile chip separation of some samples to verify the impact of compressions on separation interface and possible crack initiation. A red dye penetrant was applied to the gap by capillary action prior to chip separation in order to highlight any crack presence. The interfaces were then inspected by bright field optical microscopy.

IV. RESULTS AND DISCUSSION

A. Deformation of non-underfilled C4's under test load

Compression load tests were performed at ambient and elevated temperatures. Fig. 6 shows representative load versus displacement curves at both temperatures for a 4.22 x4.22 mm chip size. Two regions are apparent. The ramp region is an indication of the interconnect stiffness. At ambient, the stiffness is about 1.65N/μm, which is less than the 6.50N/μm value reported by Ho et al. [9]. While fixture deformation may contribute to some extent, the discrepancy can be largely explained by the differences in specific solder joint geometries. Axial stiffness is proportional not only to Young's modulus but also to the ratio of cross-sectional area to length (A/l) of the joint. Typical BGA's, as used in [9], have an A/l of about 0.38mm while the C4's in this study had an A/l of only 0.13, supporting a 3X lower stiffness value. At 120°C, the reduction in stiffness to about 1.05N/μm is coherent with equation (1), where the Young's modulus drops with a rise in temperature. The hold region is an indication of creep behavior. With constant load, there is an increase in the displacement of the package. Consistent with equations (4) and (5), creep behavior appears more prevalent at the higher temperature.

The die topology before and after a 7.6MPa normal angle compression test can be seen in Fig. 7.
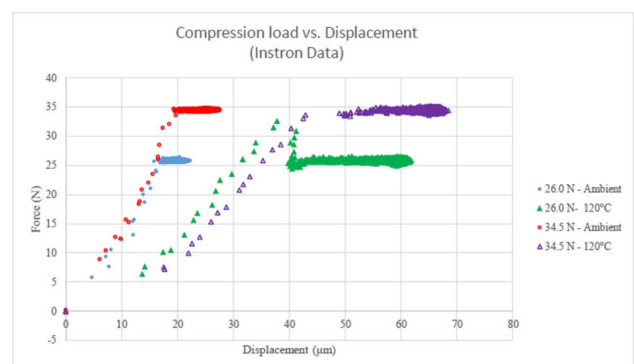

Figure 6. Compression load vs. displacement at ambient and elevated temperature.

At both ambient and elevated temperature, there is a slight tendency to flatten out. A 3D mapping of the substrate topology is shown in Fig. 8. While some change is noted after a force was applied to the die, the substrates tended to retain their shape. Fig. 9 shows the die topology before and after a 7.6MPa tilted load test. The change in the angle of the die is evident and anticipates an important change in the state of the C4 interconnections.

Joint heights before and after test compression were measured at the edges of the chip. The averages of maximum height variation per chip are shown in Table III. Under normal compression, only slight reductions in height were observed and did not tend to vary significantly with chip size or load, considering a 1.5 μm accuracy in the measurement technique. The results are coherent with an ambient yield strength of about 48 MPa.
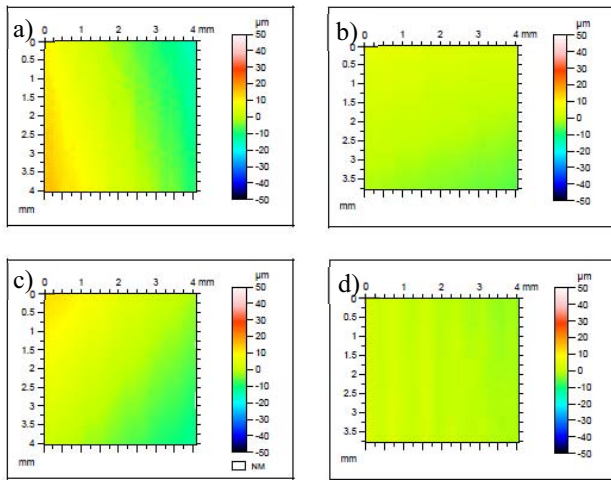
Figure 7. Topology of dies before and after a 7.6MPa normal angle compression test: a) Pre-test at ambient temperature; b) Post-test at ambient temperature; c) Pre-test at 120°C; d) Post-test at 120°C.
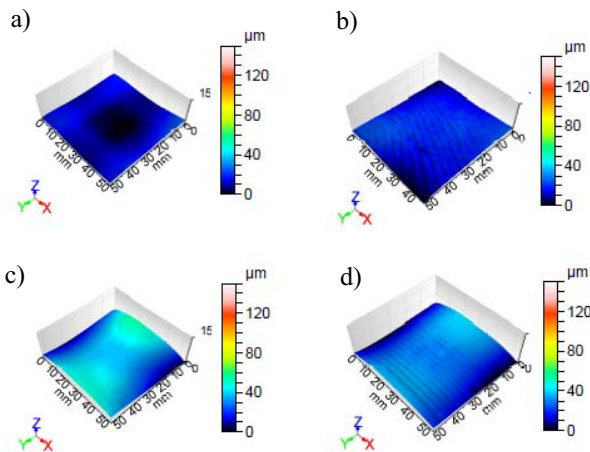
Figure 8. 3D view of the topology of substrates before and after normal angle compression test: a) Pre-test at ambient temperature; b) Post-test at ambient temperature; c) Pre-test at 120°C; d) Post-test at 120°C.

TABLE III.   AVERAGE HIGHEST JOINT HEIGHT VARIATION BETWEEN PRE-TEST AND POST-TEST COMPRESSION

| Angle | | Average max. joint height variation (μm) | | | |
| Temperature | | Normal | | Tilted | |
Pressure (MPa)	Chip size (mm)	Ambient	120°C	Ambient	120°C
7.6	4.22	6.7	7.4	-	34.9
	8.48	3.9	7.9	14.2	23.9
	12.75	-	7.0	-	15.1
	17.03	-	6.2	-	13.9
	21.30	-	5.9	-	11.8
10.2	4.22	4.6	5.7	13.1	48.1
	8.48	-	7.2	29.3	-
	12.75	8.4	7.8	-	-
	17.03	5.9	4.2	-	-
	21.30	5.9	3.3	-	-
12.5	4.22	-	-	-	59.5
15.4	4.22	-	8.5	-	-
17.9	4.22	-	-	-	36.9
20.3	4.22	-	-	-	41.7
23.7	4.22	-	-	-	40.1
25.4	4.22	-	-	-	38.5
28.1	4.22	-	-	-	37.5

However, at 120°C, where the yield strength is approximately 12 MPa, deformation would be expected to increase at loads exceeding this threshold. However, it must be considered that the load pressure was calculated as a function of the 100 μm nominal diameter of the C4 whereas the compression progressively increased the diameter, thereby lowering the true pressure. For example, cross-sections have shown diameters as large as 115 μm for a 10 μm reduction in height. With this consideration, a nominal pressure of 15.4 MPa would in fact translate to a true pressure much closer to 12 MPa.

On the other hand, joint heights under a tilted compression load exhibited strong variations, ranging from 10 μm to as much as 60 μm. While increases in load did not seem to increase the magnitude of deformation, chip size had an appreciable impact, which may be explained as follows. The load applied on a corner or a side of the chip causes it to pivot along an axis whose position depends upon the degree of load localization; C4's on one side of the axis are compressed while those on the opposite side are stretched.
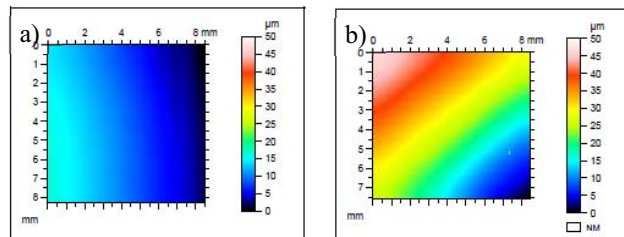
Figure 9. Topology of dies before and after a 7.6 MPa tilted angle compression test at ambient temperature: a) Pre-test b) Post-test.

The larger chip sizes present progressively greater numbers of C4s on the opposite side to counterbalance the load, hence inducing less deformation.

To complement the afore-described peripheral measurements, X-ray 3D tomography was performed on selected 4.22mm chips before and after compression to obtain a greater understanding of deformation behavior across the span of the chip. As seem in Fig. 10a, typical joints prior to any compression have the expected barrel-like shape and heights of about 65µm. Once compressed at normal angles and under ambient (Fig. 10b) or elevated (Fig. 10c) temperature conditions, the same joints maintain a similar shape, but with heights reduced to about 55 µm. On the other hand, the joints under tilted load, as shown after a 120°C compression in Fig. 10d, exhibit shapes that are a function of their position on the chip relative to the location of initial load contact; joints in the region subject to initial contact were significantly flattened (26 µm height shown) while C4's in the opposite corner have stretched (76 µm height shown) to form columnar or even hour glass structures.

The previously described Instron data suggested the existence of creep behavior within the compressed solder joints. To confirm this behavior and compare to previous studies, the measured height deformation data was plotted against load as shown by the data points in Fig. 11 at ambient and in Fig. 12 at 120°C.

The strain rates $\dot{\epsilon}$ of this study were calculated by dividing the measured height variations Δh by the nominal height h of 60 microns and the hold time t:

$$\dot{\epsilon} = \frac{\Delta h}{ht} \qquad (6)$$

The lines in each figure were plotted by applying the constants of Table I to equations (4) and (5). The dotted line is the Garofalo model without IMC while the full and dashed lines are the Garofalo 28 nm radius and 30 nm radius Ag$_3$Sn models respectively. The dash-dotted line is the Weertman two-term power law model. The data appear to fall within ranges predicted by these curves with some ambient temperature data offset at the lower stress levels and some 120°C data offset at the higher stress levels. Accuracy of this data is limited by the absence of means, such as sensors, to assess individual C4 stress as well as by the resolution of the microscope which, at 0.1 µm, limited log strain rate calculations to $10^{-5.85}$; a better resolution could result in lower values for certain data points. Further, as previously mentioned, the load applied is calculated from the nominal diameter of the C4. Correction of the data to account for progressive diameter increase and resultant decrease in true stress would tend to shift the data slightly towards the left. Finally, in the case of extreme compression such as that achieved through the tilted angle load, the C4 joints may have achieved maximum deformation prior to the end of the hold time. According to equation (6), this would increase strain rate and hence shift certain data points upwards.

Figure 11. Creep behavior of samplse versus constitutive equations at ambient temperature.

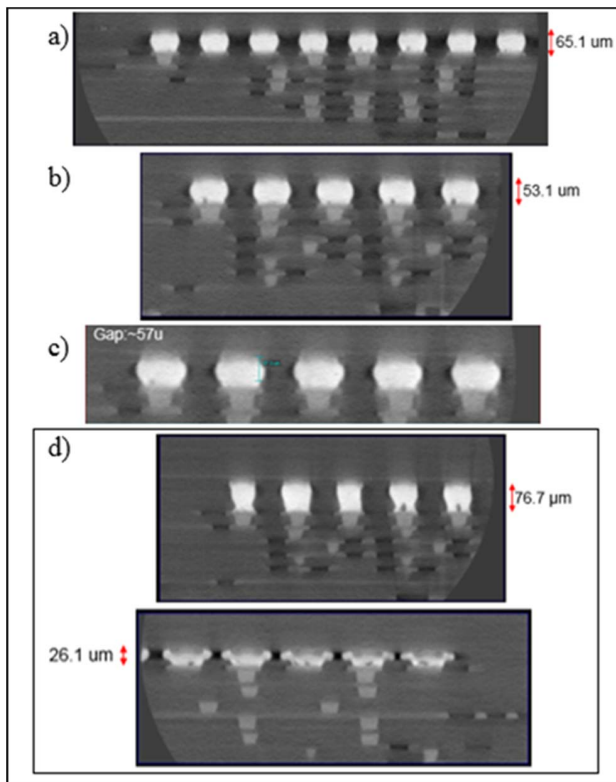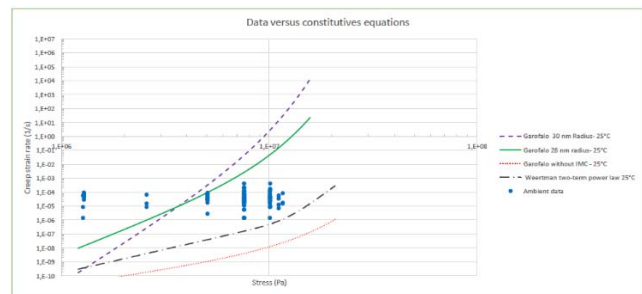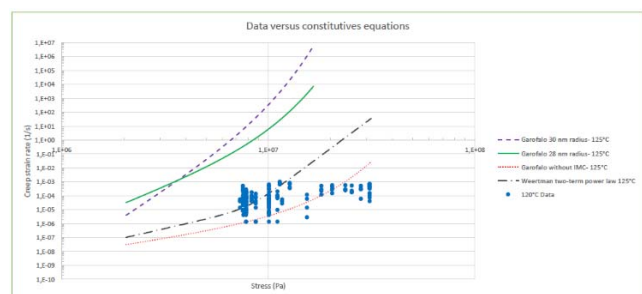Figure 12. Creep behavior of samples at 120°C versus constitutive equations at 125°C.

Figure 10. X-Ray 3D Tomography-virtual cross-sections of: a) joint without load; b) joint with normal angle load, ambient temperature; c) joint with normal angle load, 120°C; d) joint with tilted angle load, 120°C.

In order to accurately predict whether a particular constitutive relationship best represents the obtained data, future work is planned to quantify these sources of errors then compare the probable shifts to the curves by best fit analysis.

To further refine this characterization, future work is planned using nanoindentation with nanoscale accuracy on C4 size solder joints. This will allow the determination of a more relevant activation energy constant and stress exponent value which can be used to adjust the plots.

B. Interconnection integrity of non-underfilled C4's after test

Fig.13 shows the results of CSAM inspection at the various interfaces before and after compression. Neither the C4 interfaces (chip and laminate) nor the ULK layers exhibited any cracking or delamination through this inspection. The shadow-like anomalies visible in the figures were confirmed as artifacts of water movement during CSAM examination as a result of the absence of underfill in these tests.

Tensile chip separations were performed and included the use of pre-dispensed red dye to highlight any cracks that may have occurred after compression testing. Fig. 14 shows a representative tensile chip separation under normal angle load; the interfaces show consistent diameters across the chip with no defects observed.
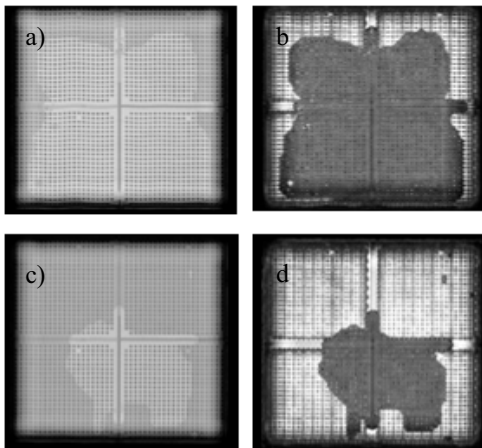

Figure 13. CSAM results:. a) Chip/C4 interface pre-test; b) Laminate/C4 interface pre-test; c) Chip/C4 interface post-test; d) Laminate/C4 interface post-test.
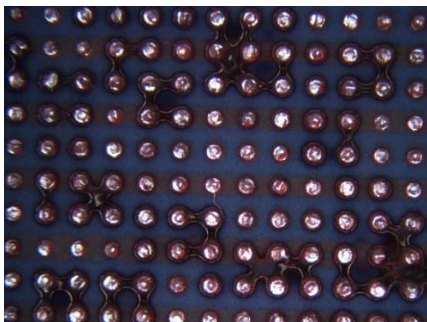

Figure 14. Tensile chip separation with red dye on a chip subjected to normal angle load.

In the case of a chip under tilted angle load, some indications of necking are observed in the region furthest from initial load contact (Fig. 15a) while diameters in the region of initial load contact progressively increase towards the corner to the point of possible bridges within the optical microscopy resolution limits, which would present a yield risk.

On the other hand, as was the case for normal angle loads, separation was consistently within the solder and no pre-separation cracking was revealed in the samples subjected to red dye.

A number of C4 cross-sections were undertaken at the various conditions of temperature and load, as shown in Fig. 16. For each case, the left and right images are representative corner C4's while the middle edge C4's are depicted in the center. Reference C4's (Fig. 16a) correlate to the previously described X-ray Tomography inspections, with slightly barrel-type shapes and heights representative of a reflow joining process.
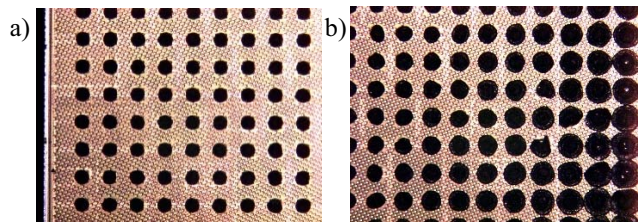

Figure 15. Tensile separation (non-red dye sample shown) on a chip subjected to tilted angle load. a) Left side of the chip; b) Right side of the chip.
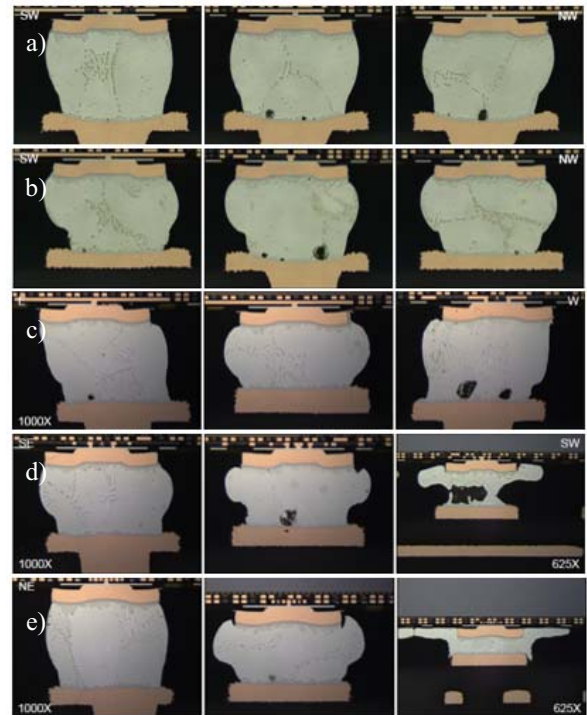

Figure 16. C4 cross-section. a) Typical joint, no pressure applied; b) Normal load, ambient temperature; c) Normal load, 120°C; d) Tilted load, ambient temperature; e) Tilted load, 120°C.

C4's under normal angle load at ambient temperature and 120°C (Fig.'s 16b and 16c respectively), while confirming a slight deformation, do not exhibit any other noticeable defect. Finally, cross-sections of C4's subjected to the tilted angle load not only confirm the deformation (compression and stretching) observed by XYZ measurements and X-ray tomography, but also reveal defective situations. Fig. 16d shows that cracking occurred on a C4 receiving the most severe height reduction during tilted ambient load; such cracking was not detected in the limited tensile pull surface characterizations and may or may not repair itself during subsequent reflow operations such as BGA attach, thereby presenting a reliability risk. Fig. 16e shows severely reduced spacing (~2μm) between adjacent C4's after the elevated temperature tilted load; subsequent underfilling may not penetrate this gap and therefore represents a risk of solder bridging during subsequent reflow operations. These occurrences support the stringent practice in actual electrical testing of controls that avoid any possibility for tilt during compressions.

Cross-sections were also observed under cross-polarized light. As previously mentioned, C4 interconnects typically have very few grains; this was confirmed to be the case in the as-joined interconnects of this study, as shown in Fig. 17a where three grains are observed. C4's that were slightly deformed (less than 10 μm) at both ambient (Fig. 17b) and elevated (Fig. 17c) temperatures also display a similar grain structure. On the other hand, C4's that were significantly deformed (more than 20 μm) at either ambient (Fig. 17d) or elevated (Fig. 17e) temperatures exhibit a greater number of grains (about 10) that appear to be randomly oriented and equiaxed. This suggests that the more deformed C4s, whose internal energies would have increased as further crystal defects (e.g. dislocations and diffusion) occurred, subsequently underwent some recrystallization to lower their energy. This is somewhat expected in that recrystallization is known to occur above $0.4T_m$ [8] and the SAC alloy is at about 0.6 T_m at ambient and almost 0.8 T_m at the elevated load temperature.

In order to observe the impact of subsequent processing of tested assemblies with respect to deformed joint behavior, some parts were submitted to underfill then BGA reflow followed by cross-sectional analysis. Slightly deformed C4s were compared to those with more important deformation. The C4s with little deformation (Fig. 18a) showed the typical 2-3 large grain structure representing a reflowed solder joint of this size. On the other hand, a third of the more deformed C4s still exhibited some degree of recrystallization, as seen in Fig. 18b, rather than reverting to their original 2-3 grain structure as could be expected after BGA reflow. This suggests that deformation, depending upon its severity, can result in a non-reversible change in grain structure in the final shipped package.
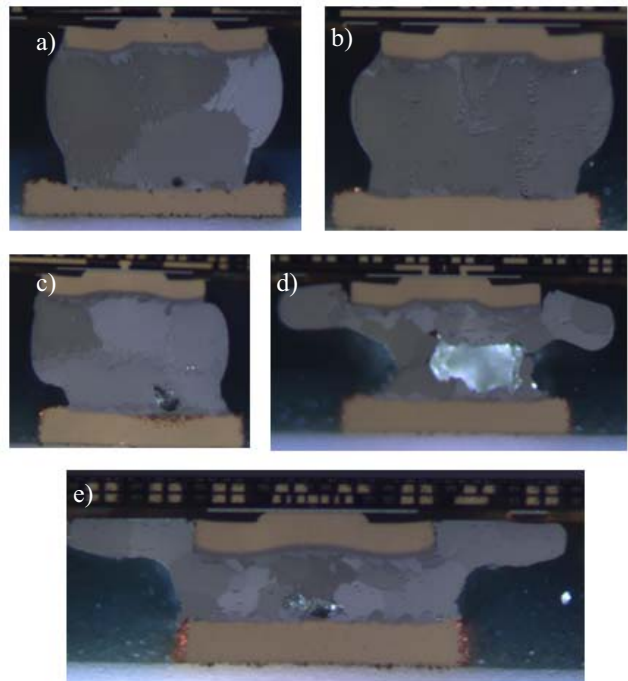

Figure 17. Cross-polarized microscopy. a) Typical joint-No deformation ; b) Slightly deformed (4.5μm) at ambient temperature; c) Slightly deformed (7.5μm) at 120°C; d) Deformed (29.3μm) at ambient temperature; e) Deformed (59.5μm) at 120°C.
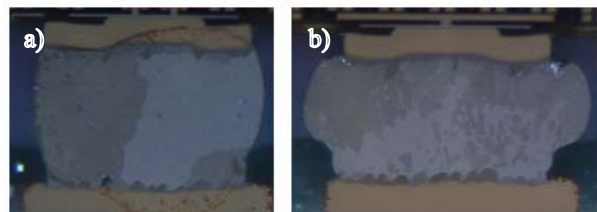

Figure 18. Microstructure of a C4 after a BGA reflow under cross-polarized light. a) Slightly deformed (3.1μm); b) Deformed(15.7μm).

While such change is expected to have negligible impact to field performance in the presence of underfill, this and previous observations of structural changes warranted reliability validation.

To this end, package assemblies were also evaluated by Deep Thermal Cycling (DTC) reliability stress testing. Table IV reports the results for the previously described groups of parts. Despite the differences in test compression simulation conditions, none of the parts exhibited an electrical fail condition, defined as measured resistance variation exceeding 20%, through pre-stress (t_0), preconditioning (t_p) and up to 1000 DTC cycles. Nevertheless, given the limited number of parts subjected to tilted angle load, further work is recommended to stress and characterize any possible reliability impacts of this condition.

TABLE IV. RELIATBILITY READ-OUT RESULTS

Read-out time	Number of defects per read-out				
	Cell A	Cell B	Cell C	Cell D	Cell E
Quantity	8	5	1	5	1
Test Conditions	None	120°C - 20 minutes Normal angle	120°C – 20 minutes Tilted angle	Ambient – 10 minutes 120°C – 10 minutes Normal angle	Ambient – 10 minutes 120°C – 10 minutes Tilted angle
t_0	0	0	0	0	0
t_P	0	0	0	0	0
t_{250}	0	0	0	0	0
t_{500}	0	0	0	0	0
t_{750}	0	0	0	0	0
t_{1000}	0	0	0	0	0

V. CONCLUSION

The effects of compression loading of non-underfilled, bare die was investigated to understand the behavior and risks related to Pb-free interconnects exposed to such conditions during electrical test of MCM assemblies prior to rework operations. It was shown that creep behavior is present at both ambient and elevated temperatures and appears to fall within the known constitutive equations. However, future work to quantify the identified sources of error is necessary in order to determine by best-fit analysis whether a particular constitutive relationship is favored.

Under normal angle loads, deformation is limited to about 10% of the original reflowed interconnect heights and showed no evidence of package integrity degradation at both the completed package level and after 1000 hours of DTC testing. On the other hand, tilted angle (<3.3°) loads can induce significant deformation of interconnects in smaller chips (<8mm) to the point where defects such as cracking (ambient load) or bridging (elevated load) could occur. Microstructures of the more deformed C4s under tilted load show signs of recrystallization to fine grain structures that would not necessarily revert to their original state after BGA reflow. Despite the degree of deformation, no impact to reliability was observed through 1000 cycles of DTC, but additional testing at tilted loads are recommended.

This study demonstrates that the angle of compression is a more important variable than load force or temperature with respect to deformation of Pb-free C4 interconnections during the electrical test of small bare die, and therefore supports the stringent use of robust manufacturing controls during such testing.

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