Optoelectronic Chip Assembly Process of Optical MCM

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***Abstract*—Assembly process reliability for Optical Multi-Chip Modules (MCM) is studied and improved. In the optoelectronic (OE) chip assembly for the Optical MCM, the OE chip with Au stud bump is joined with Sn-Ag-Cu (SAC) soldered in a through-waveguide via on an organic substrate to obtain high optical coupling efficiency. Since solid-liquid diffusion of Au to molten SAC is rapid, and formation of brittle intermetallic compounds such as $AuSn_4$ is observed by an energy-dispersive X-ray analysis, and as a result the temperature and the dwell time for the chip assembly process should minimized. Furthermore, if OE chips are underfilled, resin could infiltrate into the total internal reflection mirror cavity, and it will not reflect anymore. On the other hand, Au - SAC joints are not mechanically stable without underfill because of a large thermal stress from the coefficient of thermal expansion mismatch between the OE chip and the optical waveguide-integrated organic substrate. The issue is solved by using sidefill encapsulation instead of underfill. Appropriate material selection of a high viscosity and high thixotropic index prevented infiltration under the chip. The effect of the sidefill process is verified by simulation and experimental results. The chip assembly with sidefill passes more than 1500 deep thermal cycles from -55 °C to 125 °C.**

Keywords-Optical MCM; optical interconnetcts; waveguide; assembly; reliability; flip-chip; sidefill; underfill; adhesive material; Au stud; SAC

I. INTRODUCTION

The bandwidth requirement for high performance computing (HPC) is increasing in parallel with the performance [1]. Moreover, it will increase in wider area for various IT trends such as cognitive computing, big data analytics and cloud as a service. To meet the bandwidth requirement in computing systems, we have developed high-bandwidth density and low-power Optical Multi-Chip Modules (MCMs). The Optical MCM is an optical waveguide integrated-organic substrate on which bare optoelectronic (OE) chips are mounted close to the CPU, and incorporates 348 channels of optical I/O extending to the perimeter of the module body. Power consumption is minimized by reducing electrical wiring, while high density is achieved by the bare OE chips integration and the development of small size 24-channels microlens array with 5 x 2 mm^2 [2]. In our previous works, we demonstrated more than 30 Gbps data throughput per optical channel and 15 $Gbps/mm^2$ of bandwidth density was achieved [3].

For commercialization of the high bandwidth density and low power optical technology, it should be highly reliable and pass a qualification test. Mechanical and thermal reliability for each optical component such as organic optical waveguides and microlens arrays have been improved by sustained development. An assembly process for the Optical MCM must also have high reliability. In this paper, the developed process for OE chip assembly and its reliability are discussed.

II. OE CHIP ASSEMBLY PROCESS

Figure 1 shows an overall view of the fabricated Optical MCM [3]. A CPU chip and multi OE chips including vertical cavity surface emitting laser (VCSEL) and photodiode (PD) are integrated on the waveguide-integrated organic substrate. One layer of the optical waveguide laminated on the substrate has 25 μm core and 24 channels with 125 μm pitch in each lane.

Figure 2 shows the schematic cross section of the OE chip bonded on the polymer waveguide-integrated organic substrate. In the Optical MCM, the light from/to OE chip is optically coupled to/from the polymer waveguides via total internal reflection (TIR) mirrors. These mirrors are made inside the waveguide core with a 45 degree air slit ablated by a pulse laser.

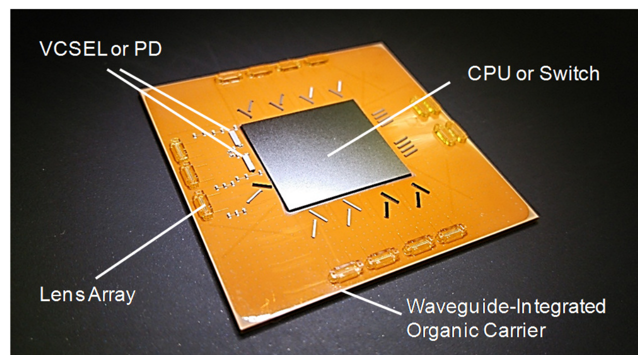

Figure 1. Overall view of the fabricated organic Optical MCM. Bare OE chips including VCSELs and PDs are mounted close to the CPU on the optical waveguide-integrated organic substrate.

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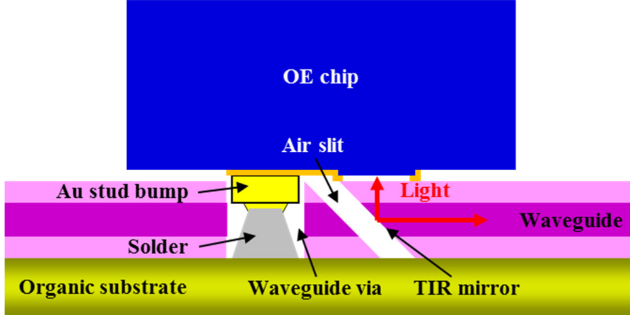

Figure 2. Schematic cross section of the OE chip assembled on the waveguide-integrated organic substrate. The OE chip attached with Au stud bumps on its bond pads is flip-chip assembled with solder deposited inside through-waveguide vias. The light from/to the OE chip is optically coupled to/from the polymer waveguides via the TIR mirror.

To reduce the optical coupling loss resulting from beam divergence, the OE chip has Au stud bumps on its bond pads and is flip-chip assembled with solder deposited inside through-waveguide vias. This benefits to minimize the distance between the OE chip and the waveguide. On the other hand, concerning the mismatch of the coefficients of thermal expansion (CTE) between the OE chip and the organic substrate, underfill resin is used to fill the gap under the OE chip for better mechanical stability after the chip bonding process. However, this possibly destroys TIR mechanism at the waveguide core/air interface once the underfill resin infiltrates into the mirror cavity. In this paper, the method for solving this issue is discussed.

Table 1 shows the data sheet of a test vehicle of the Optical MCM. The OE chip is made of GaAs. CTE of the GaAs is about 6 ppm/K [4], which is less than that of the organic substrate by about 20 ppm/K. The Au studs with a tip diameter of 25 μm are mechanically bumped on Au metallized dies using a thermosonic wire bonder which forms a Au stud size of 58 μm in diameter and 62 μm in height.

The Au stud bumps on the OE chip are dipped into a no-cleaning flux. The Au-bumped OE chip is then bonded into a corresponding via filled with SAC305. The thermal compression bonding (TCB) process is done using a flip-chip bonder at 245 °C.

Table 1. Data sheet of a test vehicle of the Optical MCM

Substrate size	50 mm x 50 mm x 1.5 mm
Substrate CTE	20 ~ 30 ppm/K
Waveguide core size	25 μm x 25 μm
Waveguide pitch	125 μm
OE chip size	3 mm x 0.23 mm x 0.15 mm
GaAs CTE	6 ppm/K [4]
Au stud diameter	58 μm
Au stud height	62 μm

A deep thermal cycling (DTC) test is carried out for reliability evaluation of the OE chip bonded substrate. Preconditioning process prior to the DTC test includes a bake at 125 °C for 24 hours, soak at 60 °C / 60 % RH for 40 hours, and three reflows at 245 °C [5]. The DTC test cycles from -55 °C to 125 °C every 15 minutes [6].

In this test, 5 channels out of 12 channels became open after one reflow process for preconditioning. Figure 3 shows a scanning electron microscope (SEM) image of one of the joints. The joint is still connected, however some cracking occurred at intermetallic compounds (IMC) of Au and SAC solder. Furthermore, the open channels are observed at both ends of the die as a result of the CTE mismatch between the OE chip and the substrate. Solutions for this issue will be discussed in the later sections.

III. JOINT RELIABILITY

Figure 4 shows energy-dispersive X-ray (EDX) analysis results of another joint after two reflow processes. Au has diffused into almost the entire solder material. The formed IMCs include AuSn, $AuSn_2$, $AuSn_4$ and others. Especially $AuSn_4$ is so brittle that cracks occurred around the IMC [7]. It is conceivable that minimizing the IMCs growth could result in higher reliability of the joint.

According to [8], the Au consumption can be used to estimate the rate of IMC formation, and follows a parabolic relationship with time. Figure 5 shows the relationship between the Au consumption versus the square root of time. The Au is consumed mainly by solid-liquid diffusion during the OE chip assembly process and reflow process for preconditioning, and also by solid diffusion at the higher temperature range of the DTC cycle. Assuming that t_1 is the time above 220 °C in the TCB and the reflow processes, and t_2 is the time spent around 125 °C in DTC, and coefficients k_1 and k_2 are Au diffusion rates for each temperature, multiple regression is performed by $x = k_1 t_1^{1/2} + k_2 t_2^{1/2}$. The steep slope

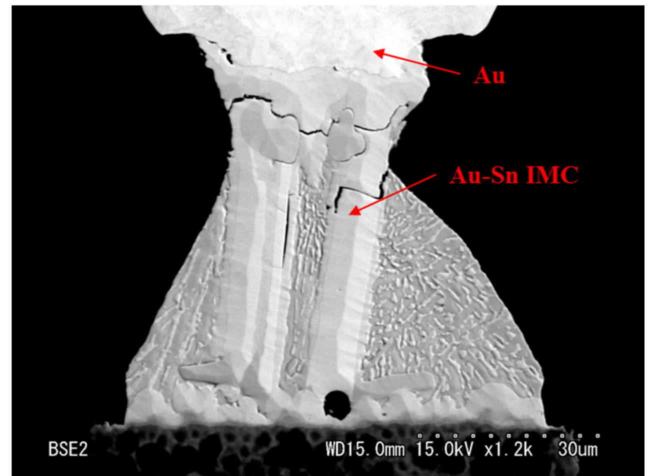

Figure 3. SEM image of an Au - SAC joint: some cracking occurred at Au - Sn IMCs.

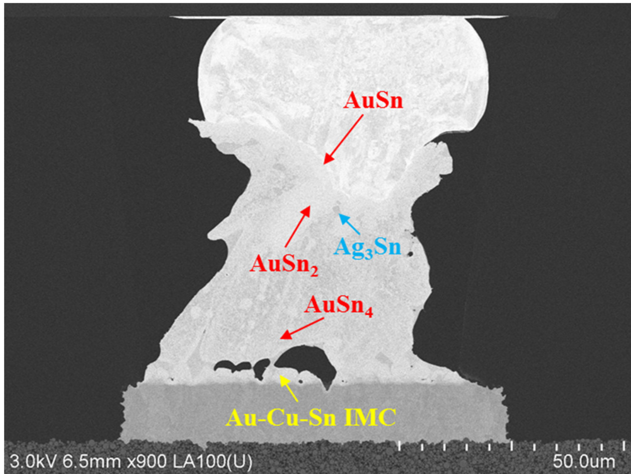

Figure 4. SEM image and EDX analysis of a joint after two reflow processes. Au diffuses into almost the entire solder material. The formed IMCs include AuSn, $AuSn_2$, $AuSn_4$ and others.

for high temperature solid-liquid diffusion is 3.8 μm/sec$^{1/2}$, and the slope for the solid diffusion is lower by more than 2 orders of magnitude. Since the solid-liquid diffusion effect on Au consumption is dominant, the chip assembly process should try to minimize the temperature and the dwell time.

IV. SIDEFILL

In terms of the CTE mismatch between the OE chip and the substrate, one reflow process for preconditioning after TCB resulted in half the number of channels opened as described above. Figure 6 shows a Au stud bump peeled off

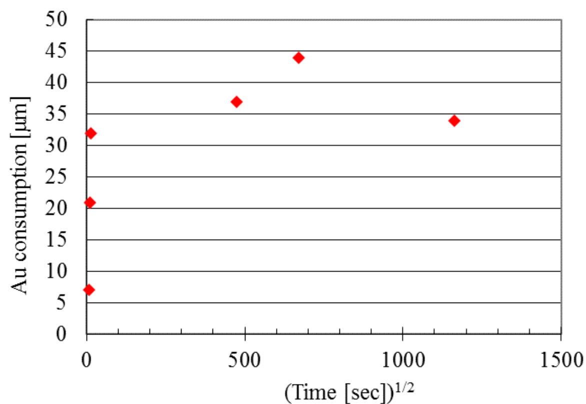

Figure 5. The relationship of Au consumption versus square root of time. Initial rapid Au consumption corresponds to solid-liquid diffusion in molten SAC during the OE chip assembly process and reflow process for preconditioning. Latter slow change corresponds to solid diffusion at the higher temperature range of the DTC cycle.

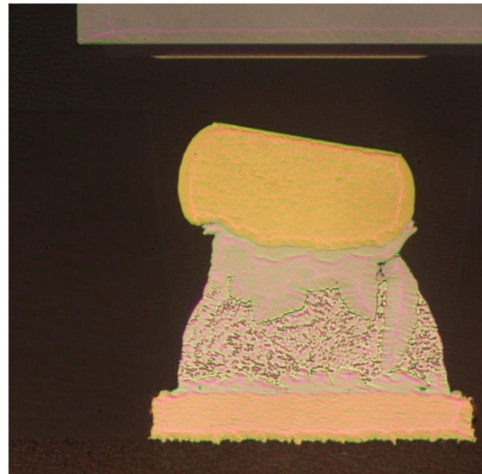

Figure 6. Au stud bump is peeled off from a chip electrode at an end channel as a result of the CTE mismatch between the OE chip and the optical waveguide-integrated organic substrate.

from a chip electrode at an end channel. In this case, we estimate that the CTE difference of ~ 20 ppm/K in a temperature change of 200 K will result in a 12 μm expansion on the 3 mm long OE chip, causing a warpage of the laminate.

We used sidefill encapsulation for solving the above mentioned issues: mechanical weakness from thermal stress resulting from the CTE mismatch, and liquid material possibly entering the mirror cavities. Figure 7 shows how the sidefill material is dispensed around the OE chip using a Musashi

Figure 7. Sidefill material is dispensed around the OE chip. Assembly yield improvement by the sidefill process has been confirmed.

Engineering digital dispenser ML-5000XII and desktop type dispensing robot SHOTMASTER300. This process is effective for assembly yield improvement and has been verified by confirming the absence of failure after three reflows.

However, depending on the materials selection, bleed-out component can infiltrate under the chip, and some cracks can still be found in the adhesive itself and in the Au - SAC joint during DTC testing. Figure 8 shows the cracks generated along Au-Sn IMCs.

Table 2 shows properties of the sidefill material used for the test vehicle. A high viscosity and high thixotropic index were considered to be appropriate to prevent infiltration under the chip. As a result of an adhesive infiltration test using a dummy substrate and a dummy chip, infiltration between the laminate and the chip is less than 25 µm, which is less than the distance between the mirror cavity opening and the OE chip edge. After the chip assembly and sidefill encapsulation using this material, no cracks were found in the joints and no failure was observed after 1500 DTC cycles, as shown in the Figure 9.

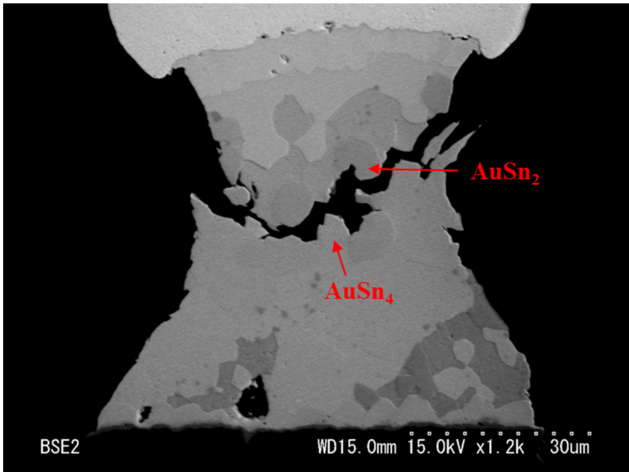

Figure 8. Crack generated along Au-Sn IMCs after 500 DTC test.

Table 2. Sidefill material properties used in this DTC test

Material	Silicone
Viscosity	304.5 Pa s
Thixotropic index	3.6
CTE	275 ppm/K
Young's modulus	3.9 GPa

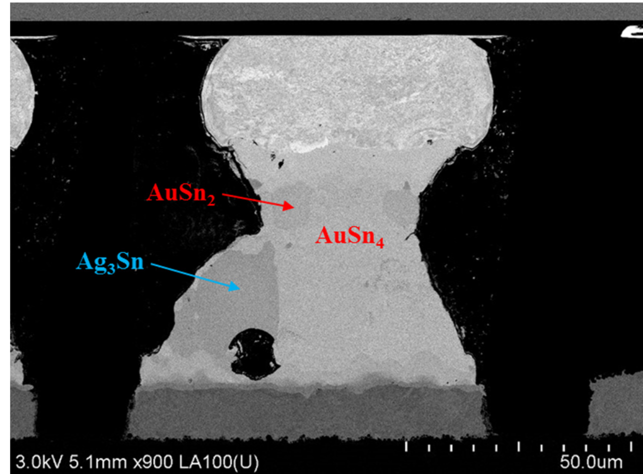

Figure 9. No failure was observed in the joints after 1500 DTC by using sidefill encapsulation.

The selected sidefill material is relatively flexible (low Young's modulus) and has a higher CTE than both the OE chip and the substrate. Although a material with a CTE closely matched to the chip or the substrate is generally preferred to relieve thermal stress, mechanical simulation showed that a high CTE material is also effective for relieving stress on joints during the cooling and shrinking phase.

Figure 10 shows the simulation model with parameters listed in Table 3. The simulation results in Figure 11 show a 54% lower stress with sidefill by using the material with a CTE of 275 ppm/K. The warpage mechanism is depicted in Figure 12, showing that the warpage occurs during the heating cycle, and a tensile stress generated in the lateral direction, especially at the edge, will be released by a lateral shrinkage of a high CTE sidefill material. Furthermore, this addition-reaction type silicone has no curing shrinkage resulting in a low level residual stress.

Table 3. Parameters list used in the mechanical simulation of the sidefill encapsulation

Substrate size	10 mm x 10 mm x 1.5 mm
OE chip size	3 mm x 0.5 mm x 0.2 mm
Bump diameter	60 µm
Bump height	80 µm
Substrate CTE	18.5 ppm/K
Sidefill CTE	275 ppm/K
Young's modulus of substrate	25.6 GPa
Young's modulus of sidefill	3.5 GPa
Fillet width of sidefill	0.2 mm

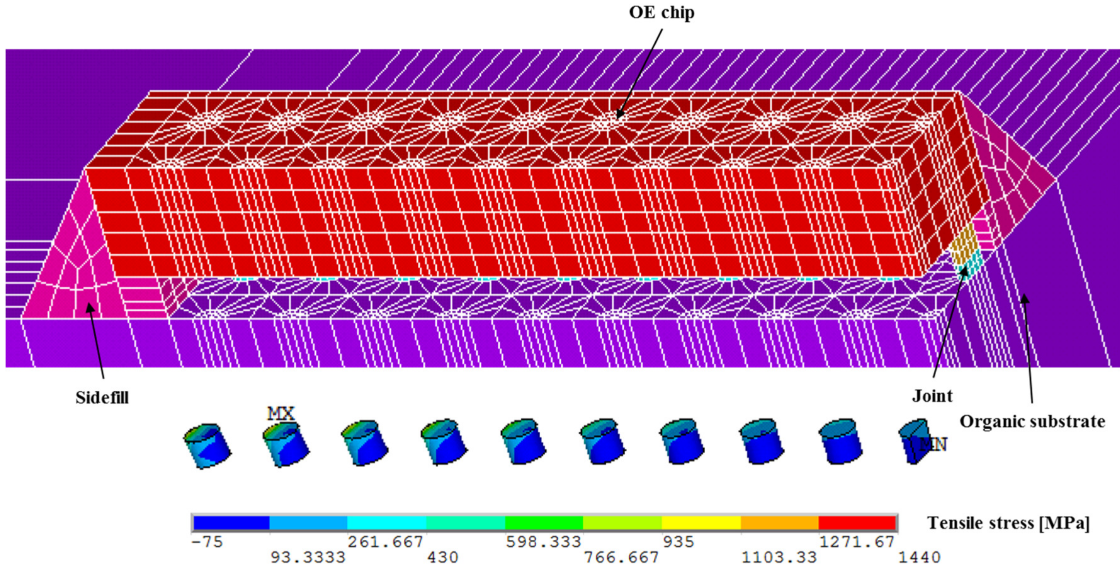

Figure 10. A model used in the mechanical simulation.

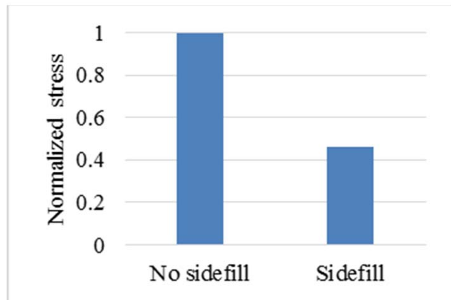

Figure 11. Simulated tensile stress at joint with and without sidefill. The results show a 54% lower stress with the sidefill material.

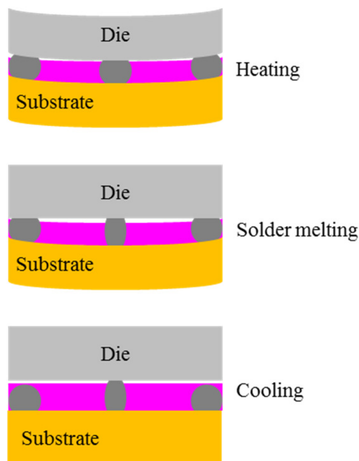

Figure 12. Warpage occurs during the heating phase, and a tensile stress is generated in the lateral direction, especially at the edge, during the cooling phase.

V. CONCLUSION

In the chip-level assembly for the Optical MCM, Au stud bump joining with SAC in the waveguide via is used to obtain better optical coupling. Au is diffused into the whole joint after the Au - SAC bonding, and IMCs such as AuSn, AuSn2 and AuSn4 are observed from the SEM / EDX analysis. These brittle IMCs caused cracks due to thermal stress during reflows and DTC using a configuration without an underfill. Since solid-liquid diffusion effect on Au in molten SAC is dominant and it leads the IMC formation, the temperature and the dwell time are minimized in the chip assembly process.

The issues are solved by applying sidefill encapsulation. An appropriate sidefill material with high viscosity and high thixotropic properties prevented infiltration under the chip. The effect of the sidefill process is verified by simulation and experimental results. The simulation results showed a 54% lower stress with a sidefill by using the material properties given in Table 2. After the chip assembly process using the sidefill material, no cracks were found in the joints and no failure was observed after 1500 thermal cycles.

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