z/OS Performance Hot Topics

Bradley Snyder
Bradley.Snyder@us.ibm.com
Agenda

- Performance and Capacity Planning Topics
  - Introduction of z Systems z13 Processor
  - Overview of SMT
  - CPUMF and HIS Support
  - zPCR Latest Status
  - zEDC
  - Flash Express/Storage
  - New RSM and WLM APARS
    • Blocked Workloads
Techdocs Website

- www.ibm.com/support/techdocs
z13 Overview

- **Machine Type**
  - 2964

- **5 Models**
  - N30, N63, N96, NC9 and NE1

- **Processor Units (PUs)**
  - 39 (42 for NE1) PU cores per CPC drawer
  - Up to 24 SAPs per system, standard
  - 2 spares designated per system
  - Dependant on the H/W model - up to 30, 63, 96, 129, 141 PU cores available for characterization
    - 85 LPARs, increased from 60
  - Sub-capacity available for up to 30 CPs
    - 3 sub-capacity points

- **Memory**
  - RAIM Memory design
  - System Minimum of 64 GB
  - Up to 2.5 TB GB per drawer
  - Up to 10 TB for System and up to 10 TB per LPAR (OS dependant)
    - LPAR support of the full memory enabled
    - 96 GB Fixed HSA, standard
    - 32/64/96/128/256/512 GB increments
  - Flash Express
IBM z13 versus zEC12 Hardware Comparison

- **zEC12**
  - CPU
    - 5.5 GHz
    - Enhanced Out-Of-Order
  - Caches
    - L1 private 64k i, 96k d
    - L2 private 1 MB i + 1 MB d
    - L3 shared 48 MB / chip
    - L4 shared 384 MB / book

- **z13**
  - CPU
    - 5.0 GHz
    - Major pipeline enhancements
  - Caches
    - L1 private 96k i, 128k d
    - L2 private 2 MB i + 2 MB d
    - L3 shared 64 MB / chip
    - L4 shared 480 MB / node
    - plus 224 MB L3 NIC Directory
Default processor assignments by POR, MES adds, and On Demand activation:
- Assign IFLs and ICFs to cores on chips in “high” drawers working down, CPs and zIIP in low
drawers working up
- Objective: Keep partitions using IFLs and ICFs “away” from z/OS partitions on CPs and zIIPs in
different drawers if possible

PR/SM assigns available memory and logical processors at activation
- Logical Processor specified in Image Profile assigned a core if Dedicated or if shared a “home”
drawer, node and chip
  • If Logical Processor becomes a HiperDispatch “Vertical High”, the Shared Logical Processor
    is assigned a specific core

Ideally assign all memory in one drawer with the processors if everything “fits”, with memory
striped across drawers with processors if memory or processors must be split
PR/SM optimizes resource assignment when triggered

- Triggers: Partition activation or deactivation or significant processor entitlement changes, dynamic memory increases or processor increases or decreases or MES change

- Optimization
  - Examine partitions in priority order by size of “processor entitlement” (dedicated processor count or shared processor pool allocation by weight)
  - Changes Logical Processor “home” drawer/node/chip assignment
  - Moves Logical Processor to different chips, nodes, drawers (LPAR Dynamic PU Reassignment)
  - Relocates partition memory to active memory in a different drawer(s) using Dynamic Memory Relocation (DMR)
    - If available but inactive memory hardware is present (e.g. hardware driven by Flexible or Plan Ahead) in a drawer where more active memory would help: activate it, reassign active partition memory to it, and deactivate the source memory hardware, again using DRM
    - PR/SM can use all memory hardware but concurrently enables no more memory than the client has paid to use
SMF 99 Subtype 14 – HiperDispatch Topology

- SMF 99 Subtype 14 contains HiperDispatch Topology data including:
  - Logical Processor characteristics: Polarity (VH, VM, VL), Affinity Node, etc.
  - Physical topology information
    • zEC12: Book / Chip
    • z13: Drawer / Node / Chip

- Written every 5 minutes or when Topology change occurs

- Topology Changes:
  - Configuration change or weight change
  - Driven by IRD weight management
  - Record provides a “Topology Change” indicator to show when the topology changed

- Recommend: Collect SMF 99 subtype 14s for ALL LPARs on the CEC!
  - Record has a single LPAR scope so need all LPARs to get total picture

- New WLM Topology Report available to process SMF 99.14 records
Example: SMF 99 z13 Topology Report

SSSS_nn_PTRYNnn
SSSS - SMFID
nn - Affinitly Node
P - Polarity (H M L)
TYP - CPU | IIP | IFL | ICF
nnn - Core ID
CPU Measurement Facility

- Available on all System z processors since z10
- Provides hardware instrumentation data for production systems

- Two Major components
  - Counters
    - Cache and memory hierarchy information
    - SCPs supported include z/OS and z/VM
  - Sampling
    - Instruction time-in-CSECT

- z/OS HIS started Task
  - Gathered on an LPAR basis, writes SMF 113 records

- Minimal overhead

- In z/OS 2.2:
  - HIS will no longer require USS definitions
  - Modify HIS (F HIS) command is restructured
### CPUMF Example Data Points

**Example built in Tivoli Common Reporting from TDSz Database**

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**z10 Only Columns**
Simultaneous Multithreading (SMT)

- Simultaneous multithreading allows instructions from one or two software threads to execute on a zIIP or IFL processor core

- SMT helps to address memory latency, resulting in an overall capacity* (throughput) improvement per core
  - Thread performance (instruction execution rate per thread) may be faster running in single thread mode
  - SMT is not available for CPs so LSPR ratings do not include it

- Capacity improvement is variable depending on workload. For AVERAGE workloads the estimated capacity* of a z13:
  - zIIP is 38% greater than a zEC12 zIIP
  - IFL is 32% greater than a zEC12 IFL

- SMT exploitation: z/OS V2.1 + PTFs in an LPAR for zIIPs and z/VM V6.3 + PTFs for IFLs

*Capacity and performance ratios are based on measurements and projections using standard IBM benchmarks in a controlled environment. Actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user’s job stream, the I/O configuration, the storage configuration, and the workload.
Simultaneous Multithreading (SMT)

- IBM z13 supports two instruction streams (threads) per core

- Threads share core resources:
  - In time: Address translator, instruction execution units, pipeline slots, …
    - Cache misses provide opportunities for other thread
    - Processor ensures fairness between threads
  - In space: Data and instruction caches, branch tables, TLBs, …
  - A thread can’t necessarily execute instructions instantly and must compete and win use of desired core resources shared between threads
  - Each thread has its own state and can do most things a core can do
    - E.g., take interruptions, start I/O, load wait PSW, signal other threads

- READY TO RUN threads share core
  - Threads NOT READY TO RUN are still unproductive while resolving cache miss
    - Core resources are productive when either READY TO RUN Thread is executing
Exploiting SMT on z13 with zIIPs

- z/OS V2R1 SMT APARs must be applied
  - OA43366 (BCP), OA43622 (WLM), OA44439 (XCF)
  - z/OS manages threads according to the SMT Mode

- Define a LOADxx PROCVIEW CORE|CPU
  - Setting is for the life of the IPL
  - PROCVIEW CORE on z13 enables SMT support

- New IEAOPTxx parameter to control zIIP SMT mode
  - MT_ZIIP_MODE=1|2
    - MT_ZIIP_MODE=2 for 2 active threads
    - When PROCVIEW CPU is specified the zIIP MT Mode is always 1
  - Update IEAOPTxx to change mode and issue SET OPT=xx command
  - Requires HD=YES, dynamic switching to HD=NO is not allowed

- New LOADxx and IEAOPTxx controls ONLY available on z/OS V2R1 and higher
RMF CPU Activity Report – zIIP CPU Activity

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<td>RPT Version: V2R1 RMF</td>
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<td>CPU: 2964</td>
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<td>Model: 736</td>
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<tr>
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### CPU Activity

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<th>CPU Activity Report</th>
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<th>LPAR Busy</th>
<th>MVS Busy</th>
<th>Parked</th>
<th>MT %</th>
<th>Util</th>
<th>Log Proc</th>
<th>Prod</th>
<th>Util</th>
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### Multi-Threading Analysis

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<td>1.000</td>
<td>1.000</td>
<td>1.000</td>
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<tr>
<td>IIP</td>
<td>2</td>
<td>1.384</td>
<td>1.225</td>
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Early SMT Testing*

*Results will vary with real online production workloads
zPCR Status

- Why use zPCR
  - LSPR Processor Capacity Ratio Tables
  - LPAR Configuration Capacity Planning

- Version C8.7g (9/15/2015)
  - The IBM z Systems (z13) processor family has been added, with 231 General Purpose models (90 sub-capacity and 141 full-speed) and 141 IFL models
  - LSPR data is now based on z/OS 2.1
  - KVM Support added as a SCP for a partition
  - New support added for Absolute Capping
  - On z13 processors SMT can be activated for z/OS running on zIIPS and z/VM running on IFLs. SMT is currently supported only by z/OS 2.1 and z/VM 6.3
  - In Advanced-Mode, the number of definable LPAR configurations has increased from 7 to 10
SMT Support in zPCR
IBM zEnterprise Data Compression (zEDC)
New data compression offering that can reduce resource usage

What is it?

✓ zEDC Express is an IO adapter that does high performance industry standard compression
✓ Used by z/OS Operating System components, IBM Middleware and ISV products
✓ Applications can use zEDC via industry standard APIs (zlib and Java)
✓ Each zEDC Express sharable across 15 LPARs, up to 8 devices per CEC.
✓ Raw throughput up to 1 GB/s per zEDC Express Hardware Adapter vs typical 50 MB a second in SW

What Changes?

It is time to revisit your decisions about compression.

- Disk Savings: Many people are already getting value from CMPSC compression and software compression today
- Performance: High throughput alternative to existing z Systems compression for large or active files.
- Industry Standard: Low cost compressed data exchange across all platforms
- Pervasive: Standard APIs allow quick adoption by middleware products running on z Systems

What is the Value?

What is the Value?

New sources of customer value

- QSAM/BSAM can save up to 4x disk space and in some cases shorten elapsed time, reducing batch windows.
- Business Partner Data Exchange can have higher throughput with lower CPU cost
- Managed File Transfer saves up to 4x link bandwidth, and up to 80% elapsed time
- ISV Products deliver expanded customer value
- Java for z/OS V7R1 accelerates common compression classes used by applications and middleware
- Improved availability with SMF
QSAM/BSAM Data Set Compression with zEDC - PTF for APAR OA42195

Reduce the cost of keeping your sequential data online
zEDC compresses data up to 4X, saving up to 75% of your sequential data disk space

Capture new business opportunities due to lower cost of keeping data online

Better I/O elapsed time for sequential access
Potentially run batch workloads faster than either uncompressed or BSAM/QSAM current compression

Sharply lower CPU cost over existing compression
Enables more pervasive use of compression
Up to 80% reduced CPU cost compared to tailored and generic compression options

Simple Enablement
Use a policy to enable zEDC compressed data sets

Example Use Cases
SMF Archived Data can be stored compressed to increase the amount of data kept online up to 4X
zSecure output size of Access Monitor and UNLOAD files reduced up to 10X and CKFREEZE files reduced by up to 4X
Up to 5X more XML data can be stored in sequential files

The IBM Employee Directory was stored in up to 3X less space
z/OS SVC and Stand Alone DUMPs can be stored in up to 5X less space

Disclaimer: Based on projections and/or measurements completed in a controlled environment. Results may vary by customer based on individual workload, configuration and software levels.
QSAM/BSAM zEDC – Value!

Better Elapsed Time
Less Data
Minimal CPU Overhead

<table>
<thead>
<tr>
<th>Data Set Type</th>
<th>Ggabytes or Seconds</th>
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<td>Extended Format</td>
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<tr>
<td>Tailored</td>
<td>10</td>
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<tr>
<td>zEDC</td>
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</table>

- Better Elapsed Time
- Less Data
- Minimal CPU Overhead

Disclaimer: Based on projections and/or measurements completed in a controlled environment. Results may vary by customer based on individual workload, configuration and software levels.
zEDC Estimation Built into zBNA (z Batch Network Analyzer) Tool

- zEDC Compression Eligible Criteria for DFSMS BSAM/QSAM Data Sets
  - Non-VSAM
  - Extended Format or Not Extended Format
  - EXCP = NO
  - Cannot be Open for Update
  - Cannot be Open with EDI processing
  - Data Set Size (Initial Allocation) >5 MB (or >8 MB if no secondary allocation)
  - Not Compressed (although could convert from Generic/Tailored to zEDC compression)

- Reports
  - Top zEDC Compression Candidate BSAM/QSAM DASD Data Sets Report includes:
    - Eligible and Extended Format
    - Eligible and not Extended Format (needs to be converted to Extended Format)
    - Eligible already Compressed (already Extended Format – required by Generic/Tailored compression)
  - Estimate of Number of zEDC Cards Required by Hour for BSAM/QSAM compression
**zEDC Top Data - with DASD Space MB Savings**

![Image of zEDC Top Data Set with DASD Space MB Savings](image-url)
Estimated zEDC Cards Report – SYS1 All Data Sets

SYS1 Est. zEDC BSAM/QSAM Demand (All DSNs)

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Estimated CPU Savings Report – SYS1 All Data Sets
z/OS V2.2 RSM Scalability Enhancements

- RSM was modified to support large amounts of real storage:
  - Initialization of real storage is more efficient
  - Management of 1MB frames is improved
  - Improvements to configuring storage online and offline
  - Steal processing can find eligible frames more efficiently

- RSM was modified to increase concurrency both at the system and application levels
  - Multiple page faults can be dealt with concurrently within an address space or with common storage
  - Page fixing and unfixing can occur concurrently within an address space or with common storage
  - Getmain/Freemain of storage can occur concurrently with page fixing/freeing and page faults
  - Less contention on available frame queues

- Rolled Down to z/OS V2.1 via APARs OA44207 and OA44436
System z and Flash Express

- **Flash Express**
  - Flash Express is a PCIe IO adapter with NAND Flash SSDs
  - Physically comprised of internal storage on Flash SSDs
  - Used to deliver a new tier of memory – storage class memory
  - Uses PCIe I/O Drawer
  - Sized to accommodate all LPAR paging
    - Each **card pair** provides 1.4 TB usable storage (2.8 TB total)
  - Supported on z/OS 1.13 plus web deliverable

- Designed for continuous availability
  - Concurrent Firmware update for service
  - RAID 10 design

- Immediately Usable
  - No capacity planning needed
  - No Intelligent data placement needed
Flash Express

- **z/OS designed to use Flash for:**
  - **Pageable large (1MB) pages**
    - With zEC12 and z13, by default there will be pageable 1 MB frames defined in storage to support hot-plugging of Flash Express cards
    - Paging, when performance would be improved vs disk-based paging
    - SVC and Standalone Dump
    - Speculative page-ins to help buffer workload spikes (such as market open)
  - **Exploiters of fixed large (1MB) pages**
    - JAVA 6 SR1 and later and its exploiters (WAS)
    - z/OS R11 and later C/C++ programs using LE
    - z/OS in z/OS R12 and later
    - IBM DB2 10
  - **Exploiters of pageable large (1MB) pages**
    - z/OS 1.13 and z/OS 2.1 Language Environment
    - Maintenance roll-up of IBM 31-bit and 64-bit SDK7 for z/OS Java Technology Edition, V7
    - DB2 11
    - IMS 12 Common Queue Server with APAR PM66866
Relative Access Times for Different Technologies

- **CPU**: Access time < 20 ns
- **Cache**: Access time < 200 ns
- **Random Access Memory (RAM)**: Access time 5-20 micro sec.
- **Solid State Drive (SSD) Storage**: Access time 1-3 ms
- **Spinning Disk Drive**: Access time < 10 ms
- **WORM, Tape Library**: Access time in seconds
Available Frame Calculations

- Available frames are tracked in RCEAFC.
  - New IEASYSxx parm INCLUDE1MAFC changes RCEAFC calculation by including Available 1MB Frames in count.
  - Min, Max, and Average values are tracked – Minimums shown below.

\[
\text{Total Available Frames} = \text{RCEAFC}
\]

- Available 4K Pages
- Available Fixed 1MB Frames
- RCEOK + Available (Buffer)
- Available Fixed 1MB Frames
- SMF71MNF – what appears in RMF Available Frame Report
- Approximation of OK threshold for stealing
- SMF71CAM
- SMF71L7M

z/OS 2.2 will include Available Fixed 1MB Frames in both SMF71MNF and SMF71CAM.
New HiperDispatch APAR – OA47968

- HiperDispatch performance improvements of the park/unpark algorithm
  - The HiperDispatch park/unpark algorithm now considers the processor topology information of the vertical low (VL) processors
  - For IBM z13 and above hardware only the HiperDispatch park/unpark algorithm now considers the average VL processor utilization when unparking VLs due to available processor free capacity (white space)
New WLM APAR – OA44526

- BLWLINTHD enhancements
- New support for blocked workloads
  - Allows lower threshold to be set
  - Defaults remain the same
- Useful for all online environments, with little to no batch workload, and heavy use of DB2
  - Helps prevent CPU starved workloads from holding locks which impact higher priority work
- Use RMF Workload Activity Report to measure the amount of blocked workload activity

```
WORKLOAD ACTIVITY

--PROMOTED--
BLK   3.240
ENQ   0.000
CRM   0.000
LCK   0.000
SUP   0.000

Check and understand why there are CPU times in any service classes
```
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